Class Project #2: Two Stage High Dynamic Range LNA

Band: 2000 MHz
To 2200 MHz

NF=2.5 dB

$P_1 = +20\ \text{dBm}$

$+V_{cc} = 3.0\ \text{Volts @ 200 mA}$

Do not use interstage Off Chip components.
Specifications

• Frequency: 2000 to 2200 MHz
• Gain (S21): 20 dB minimum
• Noise Figure: 2.5 dB max
• P-1dB: +20 dBm
• OIP3: +35 dBm
• Match (S11, S22): -10 dB min
• Vcc=+3.0 Volts, 200 mA max
• Chip size: 2000 x 2000 microns maximum
The Work

• Determine chip Architecture
• Simulate each Stage
• Simulate the cascaded Amplifier
• Make “on chip vs off chip” component decisions. Justify all “off chip” component decisions. No interstage off chip components allowed!
• Perform layout. Maximum number of Transistor fingers per tier is 15. Always use an even number of Transistor tiers.
• Introduce layout parasitics into the simulations.
• Modify layout to achieve performance, area goals.