Class Project #1: Two Stage CDMA Handset Power Amplifier

Band: 900 MHz to 1000 MHz

$+V_{cc} = 3.0$ volts @ $I_c=1100$ mA

$G=15$ dB $P_1 = +28$ dBm

No interstage
Off chip components Are allowed

$+V_{ref}$ controls $I_c$ from 100 mA To 1100 mA
PA Specifications

- Frequency: 900 to 1000 MHz
- Gain (S21): 30 dB minimum, for DC Ic ranging from 100 mA to 1100 mA.
- P-1 dB: +28 dBm minimum at max Ic
- OIP3: +45 dBm @ Pout = +28 dBm
- Match (S11, S22): -10 dB minimum
- Vcc=+3.0 volts, Efficiency>30% (I.e. Ic<1100 mA, controllable down to 100 mA with Vref)
- Chip size: 3000 microns x 3000 microns max.
The Work

- Determine chip Architecture
- Simulate each stage
- Simulate the cascaded amplifier
- Make “on chip vs off chip” component decisions. Grade will be based on minimizing off chip components. Do not use interstage off chip comp!
- Perform layout, limit transistor fingers to 15 per tier. Use an even number of tiers in all Transistors.
- Introduce layout parasitics into the simulations.
- Modify layout to achieve the performance and area goals.