MOSFETs Overview

- Metal-oxide-semiconductor field-effect transistors (MOSFET) are the building blocks of modern VLSI circuits with the areas of applications:
  - microprocessors
  - dynamic memories
  - and so on.

- In modern VLSI circuits:
  - two types of MOSFET structures are used:
    - nMOSFETs: p-substrate with n+ source-drain
    - pMOSFETs: n-substrate with p+source-drain
  - nMOSFETs and pMOSFETs are used together and is called CMOSFETs.
A. MOSFET Device Structure

MOSFETs are four terminal devices as shown in Fig. below:

1. **Gate**: thermally grown oxide on Si-substrate with conducting electrode on the top.

2. **Source-drain**: heavily-doped regions at the two ends of the gate contacted with metal interconnects.

3. **Body**: substrate connected with metal interconnect.
Layout and Structure of VLSI CMOSFETs

NMOS

PMOS

n+ poly
Spacer
P+ poly
Gate oxide
Halo

n+ p+ n+ p+p+

STI
p-well
p-substrate

n-well

n-well

CONTACT
DIFFUSION
POLY
METAL
P—WELL
N—WELL
MOSFET Circuit Symbols

nMOSFETs

pMOSFETs

G = gate; D = drain; S = source; B = Body
B. MOS Structure - Energy Band Diagram

- Note:
  - 3 materials in contact, $E_F$ = constant like PN junctions at equilibrium.
  - currents through SiO$_2$ are very small.
  - holes $\rightarrow$ metal on contact.
  - $e^-$ $\rightarrow$ semiconductor on contact.
  - bands will bend down in silicon at the interface ($\Phi_M < \Phi_S$).
MOS Structure at Equilibrium

At equilibrium \((V = 0)\).

Note:

- Abrupt transition in \(E_c\) and \(E_v\) levels at material interfaces.

- A typical potential drop \(~ 0.6\) eV across SiO\(_2\). This depends on \(E_F\) in Si. This potential can be supported because no current flows through SiO\(_2\).

- Substantial barriers exist to current flow from:
  - \(S \rightarrow M\)
  - \(M \rightarrow S\).

- Depletion region exists near the surface because \(E_F\) near the surface is further from \(E_v\) than the bulk region.
MOS Structure - Accumulation

Applied Bias: negative voltage on Al

- $E_F$ is still constant in the Si since SiO$_2$ prevents any current flow.
- $E_F$ is closer to $E_v$ at the surface.
  $\therefore$ more holes near the surface.
  $\Rightarrow$ ACCUMULATION.

-ve

\[ E_{FM} \quad qV \quad E_c \quad E_F \quad E_v \]

Al          SiO$_2$          p-Si
MOS Structure - Inversion

**Applied Bias:** positive voltage on Al

- $E_F$ is still constant in the Si ($I = 0$).
- $E_F$ is closer to $E_c$ at the surface than it is to $E_v$.
- more e- than holes at the surface.

$\Rightarrow$ INVERSION.
MOS Structure - Surface Carrier Densities

At any point in the silicon, we can calculate the hole and e-concentrations using:

\[ p = n_i e^{\frac{q\phi}{kT}} \]  \hspace{1cm} (1)

\[ n = n_i e^{\frac{q\phi}{kT}} \]  \hspace{1cm} (2)

If \( \phi_s \) = surface potential and \( \phi_p \) = bulk potential so that the potential drop across the depletion region = \( (\phi_p - \phi_s) \), then, the surface concentrations are:

\[ p_s = N_A e^{-\frac{q(\phi_p - \phi_s)}{kT}} \]  \hspace{1cm} (3)

\[ n_s = \frac{n_i^2}{N_A} e^{\frac{q(\phi_p - \phi_s)}{kT}} \]  \hspace{1cm} (4)

Since we know \( \phi_p \) from the bulk doping, if we know \( \phi_s \) for a given applied \( V_G \), then we can calculate the e- and hole surface concentrations.
C. C – V Characteristics

(a) Accumulation: $V_G > 0$

Note:
- $e^-$ are attracted to the surface.
- The small-signal capacitance per unit area is given by:
  \[ C_o = \frac{\varepsilon_{ox}}{t_{ox}} \]
  where
  - $\varepsilon_{ox}$ = dielectric constant in the oxide
  - $t_{ox}$ = oxide thickness.
**C – V Characteristics**

(b) Depletion: \( V_G < 0 \)

- \( \text{e-} \) are repelled from the surface resulting in a depletion region.
- The small-signal depletion capacitance per unit area is given by:
  \[
  C_d = \frac{\varepsilon_s}{x_d}
  \]
  where,
  - \( \varepsilon_s \) = dielectric constant of silicon
  - \( x_d \) = width of the depletion layer.
- The total capacitance:
  \[
  C = \frac{C_o C_d}{C_o + C_d}
  \]
**C – V Characteristics**

(c) Inversion: $V_G << 0$

- Minority-carriers pile-up near the oxide-semiconductor interface.
- In strong INVERSION:
  - $x_{d_{\text{max}}} = \text{maximum width of depletion region is a constant}$,
  - $C_d = C_{d_{\text{min}}} = \text{a constant}$.
- For $V_G$ between ACCUMULATION and strong INVERSION:
  - $x_d \propto V_G^{1/2}$.
Let us consider the condition (b) depletion, then:

\[ Q = Q_G = -Q_s = -qN_D x_d \]  \hspace{1cm} (5)

where,

\( x_d = \text{width of the depletion region} \)

\( N_D = \text{donor concentration/cm}^3 \).

Assuming that \( N_D \) is independent of distance (uniform substrate doping), then from Poisson’s equation we have:

\[ \frac{d^2 \phi}{dx^2} = -\frac{\rho}{K_s \varepsilon_o} = -\frac{qN_D}{K_s \varepsilon_o} \]  \hspace{1cm} (6)

\[ \therefore \phi = \phi_s \left(1 - \frac{x}{x_d}\right)^2 = \text{Potential in silicon} \]  \hspace{1cm} (7)

where \( \phi_s = \frac{qN_D x_d^2}{2K_s \varepsilon_o} = \text{Surface potential} \)  \hspace{1cm} (8)
But from Gauss’ Law, the electric displacement must be constant across the Si/SiO\textsubscript{2} interface, so that:

\[ K_o \varepsilon_{ox} = K_s \varepsilon_s \]  \hspace{1cm} (10)

where

- \( K_o \) and \( K_s \) are dielectric constants of oxide and Si respectively
- \( \varepsilon_{ox} \) and \( \varepsilon_s \) are \( \varepsilon \)-field in oxide and in Si at the interface respectively.

Assume,

\[ t_{ox} = \text{oxide thickness} \]
\[ V_o = \text{potential across oxide} \]

Then, the applied voltage is given by:

\[ V_G = V_o + \Phi_s \]

\[ = t_{ox} \varepsilon_{ox} + \frac{q N_D x_d^2}{2 K_s \varepsilon_o} \]  \hspace{1cm} (9)
C – V Characteristics

From (10) we get:
\[ \varepsilon_{ox} = \varepsilon_s (K_s / K_o) \]  
(11)

Also, from Gauss’ Law:
\[ \varepsilon_s = -\frac{Q_s}{K_s \varepsilon_o} = -\frac{Q}{K_s \varepsilon_o} \]  
(12)

\[ \therefore \varepsilon_{ox} = -\frac{Q}{K_o \varepsilon_o} \]

Then, from (9) we get:
\[ V_G = -Q \frac{t_{ox}}{K_o \varepsilon_o} + \frac{q N_D x_d^2}{2 K_s \varepsilon_o} \]
(13)

Using (5) we have:
\[ V_G = -Q \frac{t_{ox}}{K_o \varepsilon_o} + \frac{Q^2}{2 K_s \varepsilon_o q N_D} \]
(14)
C – V Characteristics

From (14) we get:

\[ Q = \frac{K_s q N_D t_{ox}}{K_o} \pm \sqrt{\left( \frac{K_s q N_D t_{ox}}{K_o} \right)^2 + 2 K_s \varepsilon_o q N_D V_G} \]

This is the amount of charge on the metal plate or in the depletion region when the depletion is taking place.

The small signal-capacitance of the structure is given by:

\[ C = \frac{dQ}{dV_G} = \frac{K_s \varepsilon_o q N_D}{\sqrt{\left( \frac{K_s q N_D t_{ox}}{K_o} \right)^2 + 2 K_s \varepsilon_o q N_D V_G}} \]

\[ \therefore \frac{C}{C_o} = \frac{1}{\sqrt{1 + \frac{2 K_o^2 \varepsilon_o}{q N_D K_s t_{ox}^2} V_G}} \quad (15) \]

(Here, \( C_o = K_o \varepsilon_o / t_{ox} \) = Oxide cap/area)


**C – V Characteristics**

During depletion, \( C \) falls as \( 1/\sqrt{V} \).

However, when the surface inverts, \( C \) reaches a minimum value.

When an inversion layer forms, we have:

\[
\phi_s \cong -\phi_F \\
\chi_d \cong \chi_{d\text{ max}}
\]

\[
\phi_s (@ V_G = V_{th}) = \pm 2\frac{kT}{q} \ln \frac{N_D}{n_i}, \quad \begin{cases} + P \\ - N \end{cases}
\]  
\[
\phi_F
\]

\[
\chi_d = \sqrt{\frac{2K_s \varepsilon_o}{q N_D} (2\phi_F)}
\]

\( (16) \)  
\( (17) \)
Thus, the total band bending is “pinned” at $2\phi_F$. Further increase in $|V_G|$ results in more carriers in the inversion layer and essentially no more band bending.
At strong inversion,

- \( \phi_s = 2\phi_F \).
- The inversion layer width < 50 A.
- A higher \( \phi_s \) or \( \varepsilon \)-field tends to confine inversion charge closer to the surface.

Generally, inversion-carriers must be treated quantum-mechanically (QM) as a 2-D gas. According to QM model:

- Inversion layer carriers occupy discrete energy bands
- peak distribution is 10-30 A away from the surface.
C – V Characteristics – Threshold Voltage

When $x_d$ reaches $x_{d_{\text{max}}}$, $C$ reaches a minimum in the $C – V$ plot and we have:

\[ C_{s_{\text{min}}} = \frac{K_s \varepsilon_o}{x_{d_{\text{max}}}} = \frac{1}{\sqrt{\frac{4kT}{q^2 K_s \varepsilon_o N_D} \ln \frac{N_D}{n_i}}} \]  \hspace{1cm} (18)

The threshold voltage is defined as the gate voltage necessary to just reach the inversion (that is, $\phi_s = -\phi_F$, $x_d = x_{d_{\text{max}}}$):

\[ \therefore V_{th} = 2\phi_F + V_o \]
**C – V Characteristics – $V_{th}$**

\[ V_{th} = 2\phi_F + t_{ox}\varepsilon_{ox} \]

\[ = 2\phi_F + t_{ox} \frac{K_s}{K_o} \int_{0}^{x_{d_{max}}} \frac{q N_D}{K_s \varepsilon_o} dx \]

[use (11) for $\varepsilon_{ox}$ and expression for $\varepsilon_s$]

Now, using the expression for $C_o$ and (17) for $x_{d_{max}}$ we get:

\[ V_{th} = 2\phi_F + \sqrt{2q N_D K_s \varepsilon_o (2\phi_F)} \frac{C_o}{C} \]

(19)

In (19), we have assumed that $Q_I \approx 0$ at $V_{th}$.

Comparison of Ideal and the measured $C – V$ plot

![Diagram showing comparison of ideal and measured C-V characteristics](image)
**C – V Characteristics – \( V_{th} \)**

Actual C - V curves are shifted laterally from the theoretical curve due to:
- Work function difference between the metal and silicon
- \( Q_f \): charge at the Si/SiO\(_2\) interface.

\[
V_{th} = \phi_{MS} - q \left( \frac{Q_f}{C_o} \pm 2\phi_F \pm \sqrt{2q N_D K_s \varepsilon_o (2\phi_F)} \right)
\]

(20)

(assume \( Q_f \) is right at Si/SiO\(_2\) interface) + p-type substrate
- n-type substrate

Thus, by measuring a C - V curve for a particular process
- \( t_{ox} \) can be calculated from \( C_o \)
- \( N_D \) can be calculated from \( C_{min} \)
- \( Q_f \) can be calculated from the difference between the ideal and experimental curves.
\[ C - V \text{ Characteristics} - V_{th} \]

If \( V_{\text{Sub}} \) = back bias = voltage between source and body:

- \( V_{\text{Sub}} > 0 \) for nMOSFETs
- \( V_{\text{Sub}} < 0 \) for pMOSFETs.

Then,

\[ V_{th} = \phi_{MS} - q \frac{Q_f}{C_o} \pm 2\phi_F + \frac{\sqrt{2q N_D K_s \epsilon_o (2\phi_F \pm V_{\text{Sub}})}}{C_o} \quad (21) \]

\[ \therefore V_{th} = V_{th0} \pm \gamma \sqrt{2\phi_F \pm V_{\text{Sub}}} - \sqrt{2|\phi_F|} \quad (22) \]

Where

\[ \gamma = \frac{\sqrt{2q N_D K_s \epsilon_o}}{C_o} \equiv \text{body factor} \quad (23) \]
Low-Frequency $C - V$ Characteristics

If the frequency of the applied signal is lower ($<< 100$ Hz) than the reciprocal of the minority-carrier response time:

- Inversion charge ($Q_I$) is able to follow the applied signal
- $Q_I$ varies with $\phi_s$ and $C_s$ depends on $Q_I$.
  
  $\therefore C \uparrow$ as $|V_G| \uparrow$.

- At higher $|V_G|$, $C$ increases back to $C_o$. 
MOS Capacitors - Polysilicon Gates

At equilibrium ($V_G = 0$).

Note:

- $E_F$ of heavily doped n+ polysilicon is near $E_c$ which must line up with $E_F$ of p-silicon.
- $E_o$ of p-silicon is higher in $e^-$ energy than that of n+ polysilicon by $E_g/2q + \phi_s$. $\therefore \varepsilon$–field is setup from n+ to p-Si.
- Band bends downward in p-silicon causing depletion region. $\therefore \varepsilon$–field from gate to substrate.
- A voltage called flat-band voltage ($V_{FB}$) must be applied to restore flat band condition. $V_{FB} = \Phi_{ms} - Q_{ox}/C_{ox}$.
- All the C - V curves discussed before are shifted by $V_{FB}$, and the $V_G$ is:
  $$V_G = V_{FB} + \phi_s - Q_{ox}/C_{ox}.$$
MOS Capacitors - Polysilicon Depletion Effect

At Inversion ($V_G >> 0$).

Note:

- Oxide field points in the direction of accelerating negative charge, bands in n+ polysilicon bends upward.
- The surface is depleted and forms a thin space-charge region in the polysilicon layer.
- Gate depletion results in an additional capacitance in series with $C_{ox}$.
- Total $C \downarrow$. $\therefore Q_I \downarrow$ and $g_I \downarrow$.

\[
\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{silicon}} + \frac{1}{C_{poly}}
\]

$C_{poly} =$ Polysilicon depletion capacitance; $C_{silicon} =$ p-silicon capacitance due to $Q_d$ and $Q_I$. 

\[
C_{ox} \quad C_{silicon} \quad C_{poly}
\]
MOS Capacitors - Polysilicon Depletion Effect

Note:

- Capacitance at inversion, $C_{\text{inv}}$ does not return to $C_{\text{ox}}$.
- $C_{\text{inv}}$ shows a maximum value $C_{\text{max}} < C_{\text{ox}}$.
- $C_{\text{max}} \uparrow$ as the polysilicon doping concentration, $N_p \uparrow$.
- Since $N_p \uparrow \Rightarrow$ depletion $\downarrow$
  \[ \therefore C_{\text{max}} \rightarrow C_{\text{ox}} \text{ for higher } N_p. \]

Total capacitance at strong inversion is given by:

\[ \frac{1}{C} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{silicon}}} + \frac{1}{C_{\text{poly}}} \]

As $V_G \uparrow$, $C_{\text{silicon}} \uparrow$ but $x_d(\text{poly}) \uparrow \Rightarrow C_{\text{poly}} \downarrow$.
  \[ \therefore \text{Low frequency } C - V \text{ shows a local maximum at } V_G. \]
D. Inversion Layer Quantization

• Typically, near the silicon surface, the inversion layer charges are confined to a potential well formed by:
  – oxide barrier
  – bend Si-conduction band at the surface due to the applied gate potential, $V_G$.

![Diagram showing energy levels $E_0$, $E_1$, $E_2$, and the edge of $E_C$ as a function of distance from the surface.]

• Due to the confinement of inversion layer $e^-$ (in $p$-$Si$):
  – $e$- energy levels are grouped in discrete sub-bands of energy, $E_j$
  – each $E_j$ corresponds to a quantized level for $e^-$ motion in the normal direction.
Inversion Layer Quantization

• Due to Quantum Mechanical (QM) effect, the inversion layer concentration:
  – peaks below the SiO₂/Si interface
  – ≈ 0 at the interface determined by the boundary condition of the e-wave function.

• Solve Schrodinger and Poisson Eq self-consistently with the boundary conditions for wave function equal to:
  – 0 for x < 0 in oxide
  – 0 at x = ∞.
Impact of QM Effect on Device Performance

• At high fields, $V_{th} \uparrow$ since more band bending is required to populate the lowest sub-band, which is some energy above the bottom of $E_C$.

• Once the inversion layer forms below the surface, a higher $V_G$ over-drive is required to produce a given level of inversion charge density. That is, the effective gate oxide thickness, $t_{OX}^{eff} \uparrow$ by:

$$\Delta t_{OX} = (\varepsilon_{ox}/\varepsilon_{si})\Delta z$$  \hspace{1cm} (24)

• Inversion layer quantization can be treated as $\textit{bandgap widening}$ due to an increase in the effective bandgap by $\Delta E_g$ given by:

$$n_i^{QM} = n_i^{CL} e^{\frac{\Delta E_g}{2kT}}$$  \hspace{1cm} (25)

Here, $\Delta E_g = E_g^{QM} - E_g^{CL}$.

(25) $\Rightarrow n_i \downarrow$ and $n \downarrow$ due to QM effect.
E. Short Channel Effect

For short channel devices, $V_{th} \downarrow$ as $L \downarrow$.

Many researchers have attempted to analyze this 2-D problem. We will consider only the simplest approach (by Yau) to understand the basic idea of short channel effect.

Assume:
- $V_D = 0 = V_S$
- $\phi_s = 2\phi_F$ @ $V_G = V_{th}$ and $\phi_s$ is unaffected by short channel effect.
- $x_d = x_{dj}$

From charge conservation:

$$Q_G + Q_{ox} + Q_I + Q_B = 0 \quad (26)$$

Also,

$$V_{th} = V_{FB} + 2\phi_F + \frac{Q_B}{C_o} \quad (27)$$

where

$$Q_B = -\sqrt{2qK_s\varepsilon_o N_A(2\phi_F + V_{Sub})} \quad (28)$$
Short Channel Effect (SCE)

From first order MOS theory:

\[ x_d = \sqrt{\frac{2 K \varepsilon_o}{q N_A}} \left( 2 \phi_F + V_{Sub} \right) \]  \hspace{1cm} (29)

Now, let us assume that only the charge inside the trapezoid is supported by the gate, i.e. the junctions support the remaining charge. *(This implies that \( Q_B \) is smaller than the long channel device and therefore, for a given \( V_G \), \( Q_I \) is larger to maintain charge neutrality. And, \( V_{th} \uparrow \)).

The total charge in the trapezoid is:

\[ Q_B' L = qN_A x_d [(L + L')/2] \]  \hspace{1cm} (30)

where, \( Q_B' < Q_B \) because \( L' < L \).

\[ \therefore \text{In Eq (27), } Q_B \text{ is replaced by } Q_B' \]
Short Channel Effect

From Fig. on the right, we get:

\[
\left( \frac{L - L'}{2} + r_j \right)^2 + x_d^2 = (r_j + x_d)^2
\]

or, \[
\frac{L - L'}{2} + r_j = \sqrt{(r_j + x_d)^2 - x_d^2}
\]

or, \[
\frac{L - L'}{2} = \sqrt{(r_j + 2x_d)r_j - r_j} = \sqrt{1 + \frac{2x_d}{r_j} - 1}r_j
\]

\[
\therefore \frac{L + L'}{2L} = 1 - \left\{ \sqrt{1 + \frac{2x_d}{r_j} - 1} \right\} \frac{r_j}{L}
\]

Using (29) and (31) in (30), we can show that:

\[
\dot{Q}_B = Q_B \left[ 1 - \left\{ \sqrt{1 + \frac{2x_d}{r_j} - 1} \right\} \frac{r_j}{L} \right]
\]
Thus, if we assume that the effect of non-uniform $Q_B$ distribution can be averaged over $L$, then:

$$V_{th} = V_{FB} + 2\phi_F + \frac{Q_B}{C_o} \left[ 1 - \left\{ \frac{1}{1 + \frac{2x_d}{r_j}} - 1 \right\} \frac{r_j}{L} \right]$$

This is the desired result that predicts $V_{th}$ as a function of $L$, $r_j$ and $x_d$ (or $N_A$) for $V_D = 0$.

Note:

1) $\Delta V_{th} \propto 1/L$.
2) As $r_j \downarrow$, $\Delta V_{th} \downarrow$, shallow junctions are preferred.
3) For large $L \uparrow$, $\Delta V_{th} \rightarrow 0$ and the long channel form applies.
4) $N_A$ shows up in $x_d$ and $Q_B$. $\therefore N_A$ affects both $V_{th}$ and $\Delta V_{th}$
5) $V_{Sub}$ is included in $x_d$ as well.
Short Channel Effect

At high $V_D$, the depletion region near the drain will expand. $Q_B$ will be further reduced and $V_{th}$ decreases. This has been analyzed by Taylor (IEEE Trans. Elec. Dev., 25, p 337, 1978).

In this case, the main change is that $L_2$ is allowed to reflect $V_D$ and the region under the gate near the source and drain is now junction charge rather than gate charge (i.e. $L_3$ and $L_4 \neq 0$).

The added complexity of the Taylor’s model does permit “reasonable” estimation of $V_D$ effects on $V_{th}$. 
Reverse Short Channel Effect (RSCE)

For sub-micron devices, $V_{th}$ is found to increase first as $L\downarrow$ and then decrease with further reduction in $L$.

The anomalous $V_{th} \uparrow$ as $L\downarrow$ is due to non-uniform lateral channel doping concentration caused by:

- an enhanced diffusion of channel implant induced by the damage from S-D implant.
- boron segregation to the S-D implant regions.
RSCE due to Source-Drain Processing

0.35 µm nMOSFETs

1.0 µm nMOSFETs

2-D boron channel profile after S-D processing
RSCE due to Halo Implant

- Halo implant around source-drain extensions (SDE):
  - significantly increases the channel doping concentration as $L \downarrow$
  - causes $V_{th} \uparrow$ as $L \downarrow$ (i.e. RSCE).
RSCE due to Halo Implant

- RSCE (i.e. $V_{th}^{\uparrow}$ with $L^{\downarrow}$) for $L_{eff} < 200$ nm is due to halo implants around SDE.
- RSCE depends on halo doping concentration.
F. Narrow Channel Effect

In addition to channel length effects on $V_{th}$, small channel widths, also, affect $V_{th}$. These effects can be understood physically as follows:

![MOS cross-section diagram]

Figure shows the MOS cross-section along the channel width direction.

The depletion layer cannot abruptly change from deep to shallow. Therefore, the transition region and some spreading of field lines from gate outside $W$.

Thus, $Q_G$ supports some charge outside $W$. As a result, $Q_I \downarrow$ and $V_{th} \uparrow$. 
Narrow Channel Effect

Consider the uniformly doped substrate with $V_D = 0$.

$Q_{BW} = \text{triangle area charge under thick oxide that is supported by gate.}$

$Q_{BL} = \text{trapezoidal area charge supported by gate (Yau).}$

The parameter $\alpha$ depends on oxide thickness, shape of field oxide edge, substrate doping, field threshold adjustment implant, and so on.

It is likely that $\alpha$ has to be experimentally determined.
Narrow Channel Effect

The charge inside the volume is \((1/2)Q_{BW}\). The shape is rectangular on top, the sides are triangular and slope inward.

We know from SCE:

\[
Q_{BL} = qN_A LW x_d \left[ 1 - \left( \frac{2x_d}{r_j} \right) \frac{r_j}{L} \right] \tag{34}
\]

The charge contained in the volume above can be shown to be:

\[
Q_{BW} = \alpha qN_A LW x_d^2 \left[ 1 - \left( \frac{2x_d}{r_j} \right) \frac{r_j}{3L} \right] \tag{35}
\]

Now, we assume that the narrow width and short channel effects can be simply superimposed so that the total charge supported by the gate is given by:

\[
Q_T = Q_{BL} + Q_{BW}
\]
Narrow Channel Effect

The charge contained in the volume can be shown to be:

\[ Q_T = Q_{BL} + Q_{BW} \]

\[ = qN_A LWx_d \left[ 1 - \frac{r_j}{L} \left( 1 + \frac{2x_d}{r_j} - 1 \right) + \frac{\alpha x_d}{W} \left( 1 - \frac{2 r_j}{3 L} \left( 1 + \frac{2x_d}{r_j} - 1 \right) \right) \right] \]

\[ = qN_A LWx_d \left[ 1 + \frac{\alpha x_d}{W} - \frac{r_j}{L} \left( 1 + \frac{2\alpha x_d}{3 W} \right) \left( 1 + \frac{2x_d}{r_j} - 1 \right) \right] \tag{36} \]

The term in front of the brackets can be recognized as the bulk charge which would be present in a long and wide channel device so that:

\[ V_{th} = \phi_{MS} - \frac{Q_f}{C_o} + 2\phi_F + \frac{Q_T}{C_o} \]

\[ \therefore V_{th} = \phi_{MS} - \frac{Q_f}{C_o} + 2\phi_F + \frac{Q_B}{C_o} \left[ 1 + \frac{\alpha x_d}{W} - \frac{r_j}{L} \left( 1 + \frac{2\alpha x_d}{3 W} \right) \left( 1 + \frac{2x_d}{r_j} - 1 \right) \right] \tag{37} \]
Narrow Channel Effect

\[ V_{th} = \phi_{MS} - \frac{Q_f}{C_o} + 2\phi_F + \frac{Q_B}{C_o} \left[ 1 + \frac{\alpha x_d}{W} - \frac{r_j}{L} \left( 1 + \frac{2 \alpha x_d}{3 W} \right) \left( \sqrt{1 + \frac{2x_d}{r_j}} - 1 \right) \right] \]  

(38)

where \( Q_B \) is given by: \( Q_B = -\sqrt{2qK_s\epsilon_o N_A (2\phi_F + V_{BS})} \)

Note that if \( L \) and \( W \to \infty \), the normal long channel \( V_{th} \) Eq is obtained.

Summary:

- \( L \downarrow \Rightarrow V_{th} \downarrow \)
- \( W \downarrow \Rightarrow V_{th} \uparrow \)
- \( x_d \uparrow \Rightarrow V_{th} \) more sensitive to \( L \) and \( W \) (i.e. lightly doped substrates and/or \( V_{Sub} \) increase problems).
- \( r_j \uparrow \Rightarrow V_{th} \) more sensitive to \( L \) (i.e. deep junctions undesirable).
- \( \alpha \downarrow \Rightarrow \) minimizes \( V_{th} \) variation due to narrow \( W \).