As a device engineer, you are asked to generate SPICE (compact) model for 0.13 μm logic CMOS technology. You will be working with a fellow engineer. One of you will be responsible for the NMOS while the other will be responsible for the PMOS. You have the choice of providing your design engineering group BSIM3 or BSIM4 models. As a preparation to generate device models you need to develop a strategy so that your models characterize geometry dependence of MOSFET device performance. In this project, you will develop a complete strategy to extract compact models for 0.13 μm logic CMOS technology operating at supply voltage $V_{DD} = 1.5$ V.

(a) Select the devices (W/L) to collect I – V data for device modeling. Explain your reasoning for the range of devices selected.

(b) Select the device characteristics required to extract complete set of compact models.

(c) Create a Table to show the measurement conditions required for the device characteristics in part (b).

(d) Build a complete strategy to optimize model parameters using the device characteristics selected in part (b). Explain your reasoning, clearly.

(e) Finally, add to part (d) a strategy to optimize the temperature dependence of the relevant model parameters.

(f) Show the final model files.

Report Format:

Each engineer should turn in a report on his/her part of the strategy (i.e. NMOS or PMOS), and reference the name of the partner. Your report must be less than 8 pages long (excluding Appendix)