On-Chip Inductance: Measurement, Modeling, and Simulation

Dusan Petranovic

Abstract

In order to satisfy increasing performance requirements with continuously scaling technology, new materials (low resistivity copper metal lines and low K dielectrics) have been introduced, together with an inverse scaling of the upper metal layers. These measures have proven effective in controlling RC interconnect delay. However, all these measures also make the inductive effects more pronounced and render frequency invariant RC-based interconnect models increasingly inaccurate and inadequate. With clock rates now in gigahertz range, inductance is becoming more important and can no longer be ignored. A large portion of the wide wires encountered in global interconnects, as well as in the clock and power distribution networks, should now be treated as RLC circuits. That makes all work related to interconnect (measurement, extraction, modeling, simulation and design) much more complex. We will discuss new issues and challenges facing research community related to on-chip inductance, as well as the ways the industry (LSI logic in particular) is responding to them. The results in S-parameter measurements, in partial and loop inductance extraction and modeling will be presented. We will also discuss our initial results, obtained in cooperation with universities, in analysis of massive RLCK networks, which pose big problems for the circuit simulators as well as for the system order reduction procedures.

Dusan Petranovic received his BS in electrical engineering from University of Belgrade in 1976, and MS in computer engineering from Worcester Polytechnic Institute in Massachusetts in 1979, where he spent one year on a Fulbright Grant. He received PhD from University of Montenegro in 1986, where he was employed as an Assistant and an Associate Professor until 1992. At University of Montenegro he had been involved in developing and teaching courses in electrical and computer engineering, as well as in research in the areas of microprocessor system design, digital signal processing and control system design. Before moving to the USA, he also worked as an adjunct professor at the University of Belgrade and served as an EE department Dean and Chair at the University of Montenegro. Dusan Petranovic spent six years teaching at Harvey Mudd College in Claremont, California. He joined LSI Logic Advanced Development Laboratory as a member of technical staff in 1997, and until recently was with the Process R&D, working on the interconnect modeling for high-speed digital circuit design. He worked as a consultant for NASA on aircraft control law design, and for NOVA Management Inc. on a design of Tera FLOPS digital signal processor. He has published more than thirty international journal and conference papers and is a holder of eight U.S. patents. He has given numerous seminars and lectures including invited presentations at California Institute of Technology, University of Southern California and Imperial College of Science and Technology.