Unified Model for Deep Sub-micron On-chip Interconnects Including Non-orthogonal Architecture

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Abstract

It has been well known that the delay due to clock distribution and global interconnect has limited the I/O speed in keeping up with the core speed improvement trend. The ever-increasing gap between interconnect delay and gate delay has motivated a new non-orthogonal wiring architecture, X-architecture. In this talk, we investigate the electrical properties of the general non-orthogonal wires, introducing a scheme for modeling and parameter extraction of on-chip capacitance and inductance. In the first half of the talk, we will talk about a unified quasi-3D capacitance extraction based on a novel concept of “effective width”. This is in essence an electrostatic width of a crossover line, and it provides a way to decompose any complicated 3D structures into a series of successive 2D structures, leading to efficient capacitance extraction. The rest of the talk will be devoted to the development of an effective loop inductance model for high-frequency interconnects. Validation and extraction methodology of the effective loop inductance, which is more computationally efficient than the partial inductance approach, will be addressed. High-frequency characteristics, including random capacitive coupling and skin effect, will be investigated through a full wave solver and S-parameter based methodology, leading to a frequency-dependent RLC model valid up to 100GHz.

Biography of Speaker

Sang-Pil Sim received the B.E. degree in electrical engineering from Seoul National University (SNU), Seoul, Korea, in 1988 and the M.E. degree in electrical engineering and computer science from Korea Advanced Institute of Science and Technology (KAIST), Taejeon, Korea, in 1990. From 1990 to 1998, he was with Semiconductor Researcher & Development Center, SAMSUNG Electronics Corporation, Kiheung, where he was involved in the development of quarter micron transistor, process integration, and failure analysis engineering for yield and performance improvement of DRAM. In 1994, he received a grand prize from the president of SAMSUNG group for the contribution to the first development of 256 Mega bit DRAM in the world. In 1999, he returned to KAIST to work toward the Ph.D. degree in electrical engineering and computer science. He is currently working on interconnect modeling for high-speed digital circuit design at Santa Clara University, Santa Clara, as a visiting researcher. He is expected to receive his doctoral degree in August 2003. His research interests include modeling and device physics of RF CMOS, and high-frequency characterization and modeling of on-chip interconnects.