Class Project #2: Two Stage PCS Low Noise Amplifier

Band: 1800 MHz
To 1850 MHz

\[ \text{NF} = 2.5 \text{ dB} \]

\[ +\text{Vcc} = 3.5 \text{ Volts @ 50 mA} \]

\[ \text{P-1} = +10 \text{ dBm} \]
Specifications

• Frequency: 1800 to 1850 MHz
• Gain (S21): 20 dB minimum
• Noise Figure: 2.5 dB max
• P-1dB: +10 dBm
• OIP3: +25 dBm
• Match (S11, S22): -10 dB min
• Vcc=+3.5 Volts, 50 mA max
• Chip size: 1500 x 1500 microns maximum
The Work

• Determine chip Architecture
• Simulate each Stage
• Simulate the cascaded Amplifier
• Make “on chip vs off chip” component decisions. Justify all “off chip” component decisions.
• Perform layout
• Introduce layout parasitics into the simulations.
• Modify layout to achieve performance and area goals.