Class Project #1: Two Stage PCS Power Amplifier

Band: 1850 MHz to 1900 MHz

$P_1 = +30$ dBm

$+V_{cc} = 6.0$ volts @550 mA
PA Specifications

- Frequency: 1850 to 1900 MHz
- Gain (S21): 20 dB minimum
- P-1 dB: +30 dBm
- OIP3: +45 dBm
- Match (S11, S22): -10 dB minimum
- Vcc=+6.0 volts, Efficiency>30% (I.e. Ic<550 mA)
- Chip size: 2500 microns x 2500 microns max.
The Work

- Determine chip Architecture
- Simulate each stage
- Simulate the cascaded amplifier
- Make “on chip vs off chip” component decisions. Justify all “off chip” component decisions.
- Perform layout
- Introduce layout parasitics into the simulations.
- Modify layout to achieve the performance and area goals.