RFIC DESIGN ELEN 376
Session 6
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May 8, 2002
Definition of Noise Figure

\[ \text{NF} = \frac{<S/N \ \text{in}>}{<S/N \ \text{out}>} \]
Noise Power Output from an Amplifier with Noise Figure F

\[ P_{n \text{ in}} = kTB \]

![Diagram of an amplifier with noise figure F](image)

\[ P_{n} = FGkTB \]

\[ Z_{\text{in}} = 50 \quad Z_{\text{out}} = 50 \]
Definition of Noise Temperature

• Refer all of the LNA’s Noise output to its input, and express it as an Increase in the Source Resistance Thermal Noise, $kT_B$.

• $NF = (1 + \frac{T_n}{T_0})$, where $T_0 = 290$ Degrees K

• $T_n = T_0 (NF - 1)$

• $NF$ in dBs = $10 \ LOG \ (1 + \frac{T_n}{290})$
Total Noise Figure of a Front end Attenuation and an LNA

\[ \text{NF}_{\text{total}} = A + \text{NF(LNA)} \text{ in } \text{dBs} \]
Total Noise Figure of a Multi Stage LNA

\[ \text{NF}_{\text{total}} = \text{NF}_1 + \frac{(\text{NF}_2 - 1)}{G_1} + \frac{(\text{NF}_3 - 1)}{G_1G_2} + \ldots \]
Total Noise Temperature of a Multi Stage LNA

\[ T_{n\ total} = T_{n1} + \frac{T_{n2}}{G_1} + \frac{T_{n3}}{G_1 G_2} + \ldots \]
Dynamic Range of an LNA
APPCAD Analysis of a Two Stage LNA with .5 dB Attenuator
Physical Sources of Noise in Active Devices

- Thermal Noise: $P_n = kTB$  (All Devices)
- Shot Noise: Mean sq In = $e I_{dc} B$  (Dominates in Bipolar Devices)
- (1/F) Noise: Mean sq In = $N I_{dc} B / F$  (Dominates in FET Devices)
Frequency Behavior of Physical Noise Sources

![Graph showing frequency behavior of physical noise sources with (1/f) Noise, Shot Noise, and Thermal Noise plotted against frequency.]
Typical LNA Noise Figure Behavior with Frequency
Sources of Noise in Bipolar Devices

Shot noise occurs as carriers pass through the junctions.
Sources of Noise in an FET Device

UNDEPLETED RESISTIVE MATERIAL

GATE

SURFACE TRAPS THAT CAUSE (1/f) NOISE

SOURCE

DRAIN

CHANNEL

CARRIER

DEPLETION REGION
The Physical Mechanism Causing (1/f) Noise in FETs

Electrons are Trapped and released with a distribution of lifetimes

Slow Trapping States just Below the Conduction Band
Ultra Low Noise PHEMT Structure
Heterojunction Potential Gradient Forces Electrons from Heavy Doped AlGaAs into GaAs
Carrier Drift Velocity in GaAs Based on Scattering Mechanism

High Mobility In light doped Case leads to high Transconductance and low Noise Figure

Drift Velocity

Optical Phonon Scattering (Light Doping)

Impurity Scattering (Heavy Doping)

Electric Field
Apply Gamma opt Input Match to an Active Device for lowest Nf

Match for Max Gain

Gamma opt input Match Produces the lowest Noise Figure, at some gain Reduction

Rule of Thumb:
Gamma opt has $\frac{1}{2}$ the Magnitude of S11*, and The same angle
Low Pass Matching LNA Topology
Low Pass Matching with Parallel Feedback LNA Topology
Low Pass Matching with Series Feedback LNA Topology
Distributed Amplifier LNA
Topology: Two Sections

Q1 an Q2 are Mesfets
Or Phemts
Distributed Amplifier Design Relationships

- \( \text{Cgs} = \text{Cds} + \text{C1} \) (Drain and Gate Line Shunt Capacitance is made the same, so the delay per section is the same on each line)
- \( \text{Z0} = 50 = \sqrt{\frac{\text{L}}{\text{Cgs}}} \) (Set Gate and Drain lines to \( \text{Z0} = 50 \) Ohms)
- \( \text{Fc} = \frac{1}{\pi} \text{Z0 Cgs} \) (Cutoff Frequency)
- \( \text{Gain} = 20 \log_{10} \left( \frac{\text{N Z0 Gm}}{2} \right) \) (Gain for an \( \text{N} \) section Distributed Amplifier)
Gain Response of a Distributed Amplifier

Cutoff Frequency
Can exceed 40 GHz
With .15 micron PHEMTs
Balanced Amplifier LNA Topology

\[ \text{NF}_{\text{total}} = G \text{ coupler} + \text{NF} \]
General Recommendations for HBT LNA Designs

- Use a small, very High Gain, Device to avoid second stage contributions (compromise on device size if high dynamic range is needed).
- Set bias currents to be very low, to avoid shot noise in the junctions (compromise on current if high dynamic range is needed).
- Place input matching inductors off chip to avoid front end attenuation with lossy on chip inductors.
- If Parallel Feedback is needed for Stability, use a high value of resistance, to avoid loss.
Homework #5: An LNA Circuit using LP Match and Parallel FB
“On Chip” Circuit Details
Total Chip Layout
Blowup Near Transistor

1000 OHMS

Q1, \[ A = 1 \]

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Blowup of .70 pF Capacitor
Blowup of .80 pF Capacitor
Blowup of the 5 pF Capacitor