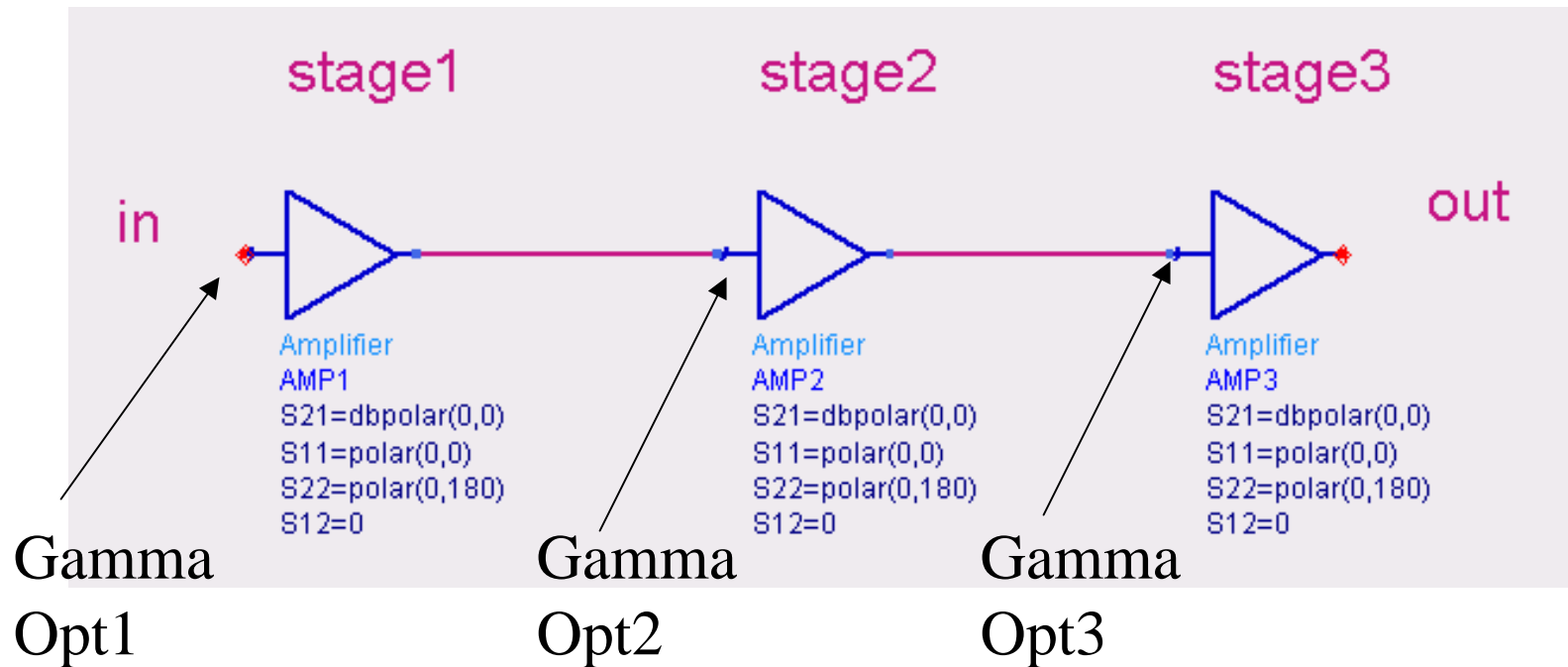


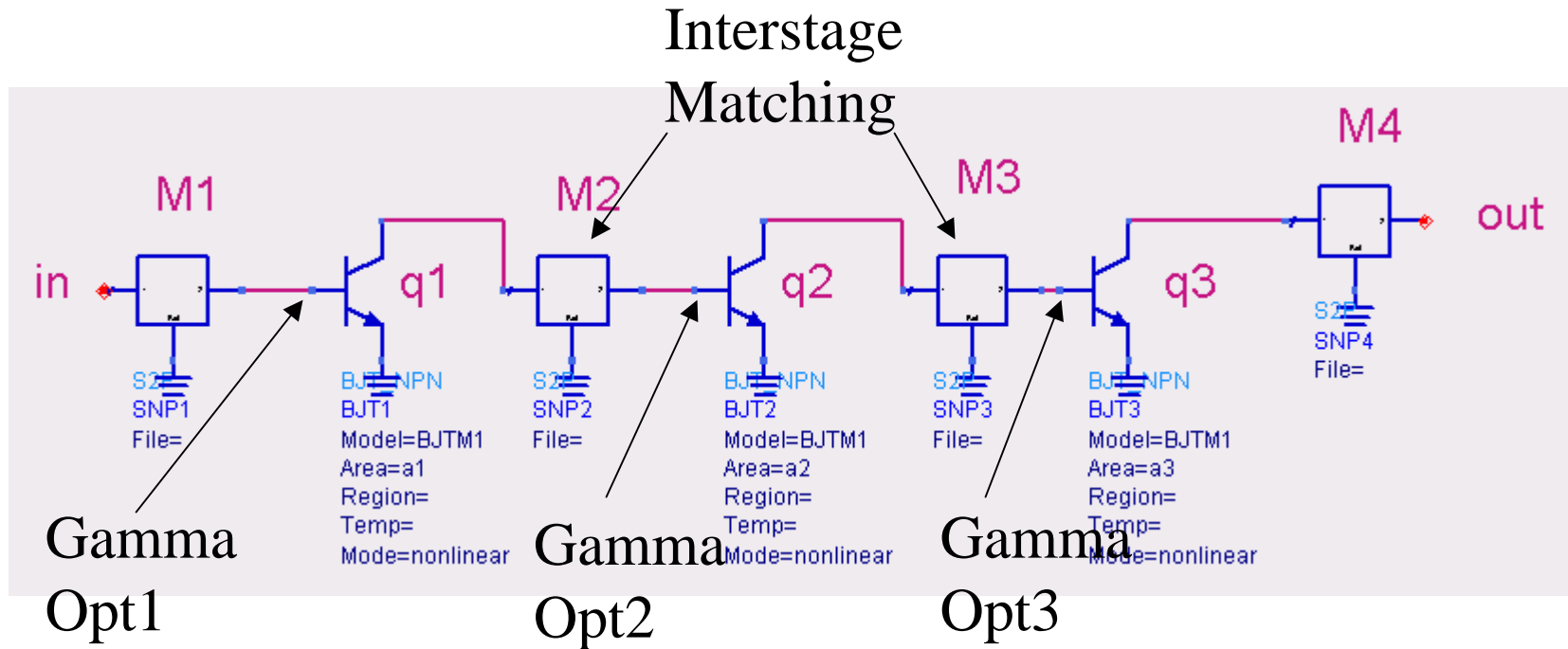
RFIC Design ELEN 351  
Lecture 6: Designing Multistage  
Amplifiers

Instructor: Dr. Allen Sweet

# Multistage LNA Design: Block Diagram level



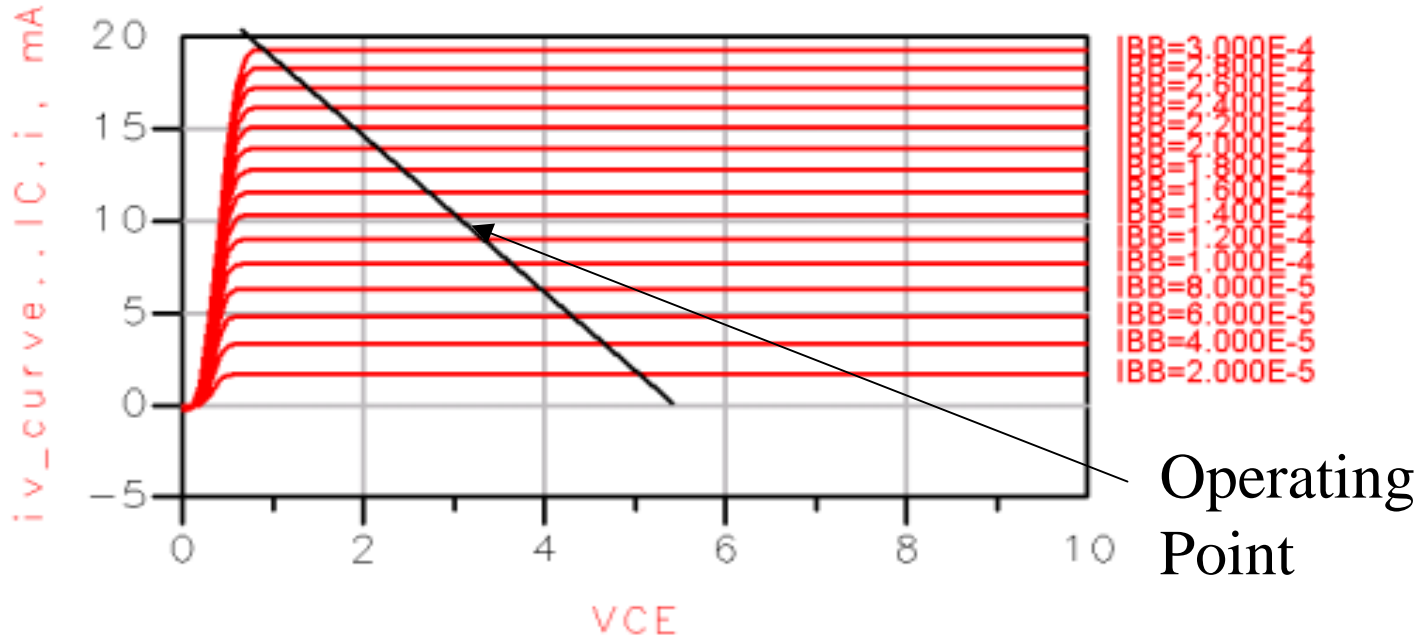
# Multistage LNA Design, Transistor Level: Start at the Input and Proceed to the Output



# LNA Interstage Performance Spreadsheet

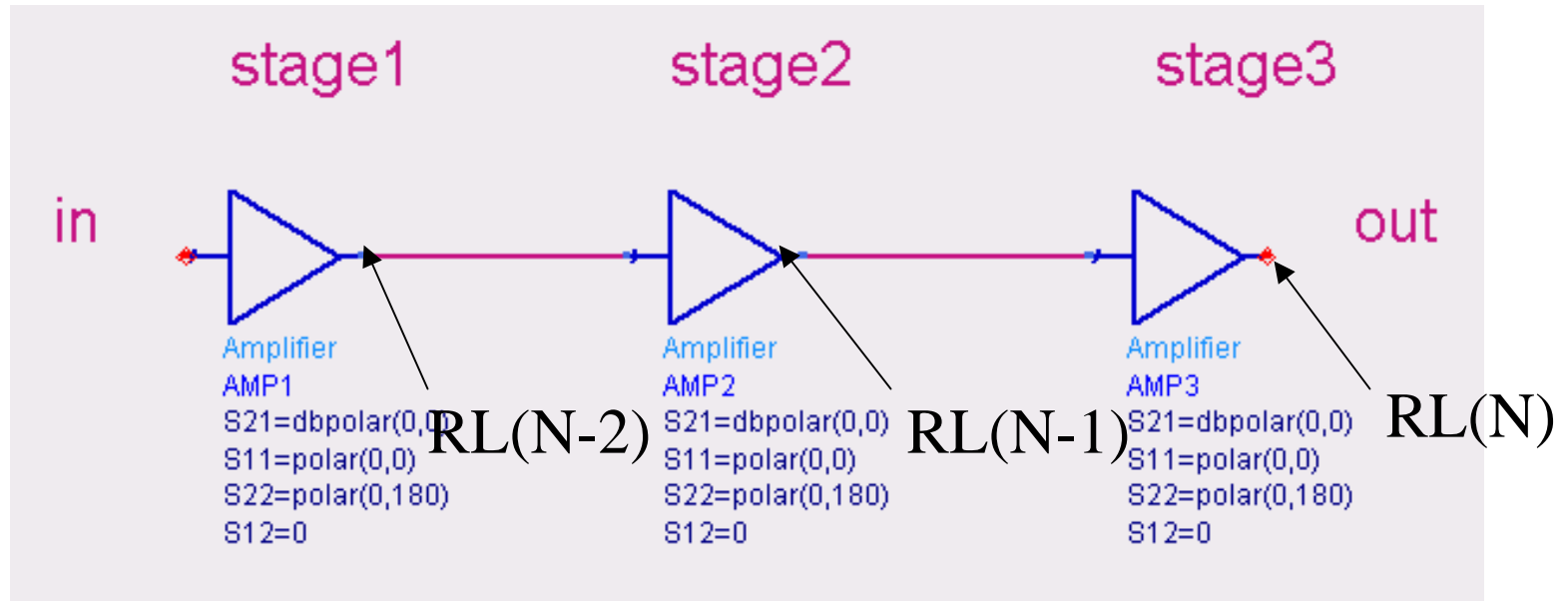
STAGE	SIZE	Ic	GAIN	GAMMAop	NF	Nfcontribution	Zin	Zout
1								
2								
3								
4								
N								

# Class A load line for a single emitter finger operating at 3 volts

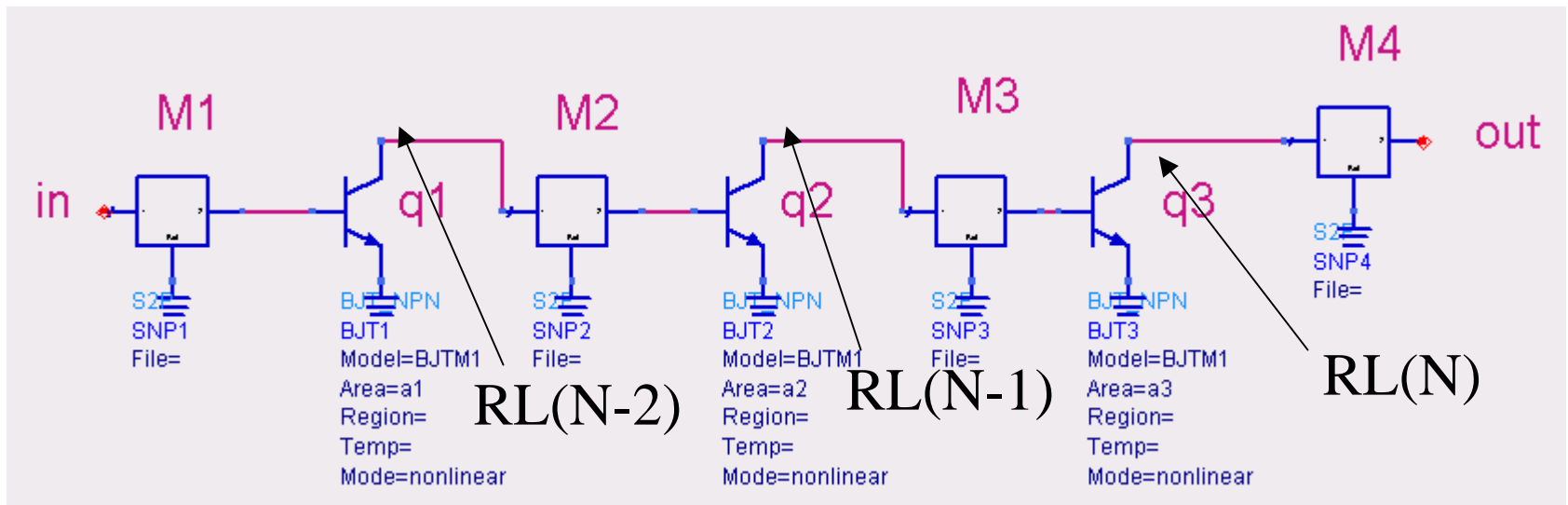


LOAD LINE FOR A SINGLE EMITTER FINGER OPERATING IN CLASS A AT  $V_{CC}=3.0$  VOLTS AND  $I_{CC}=10$  mA IS 225 OHMS PER FINGER. LOAD LINE FOR N FINGERS IS  $225/N$  OHMS

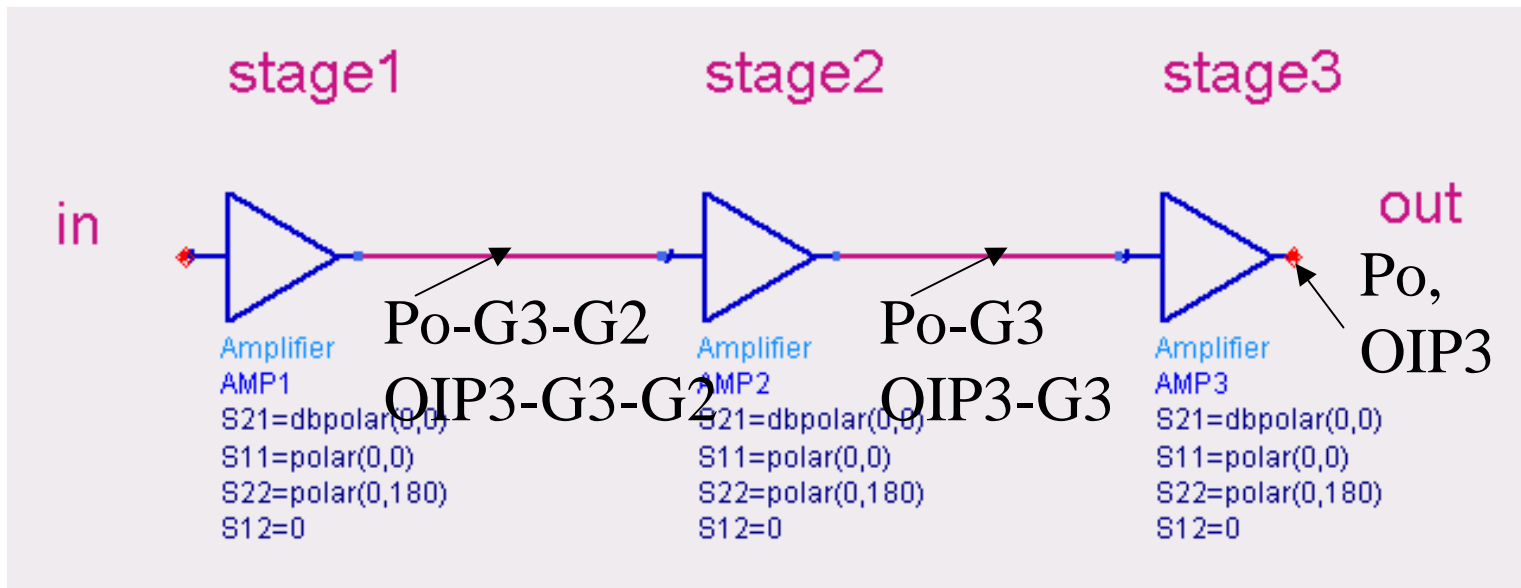
# Multistage PA Design: Block Diagram level



# Multistage PA Design, Transistor Level: Start Process at the Output and Proceed to the Input



# Calculating Power and OIP3 for each stage in a Multistage PA

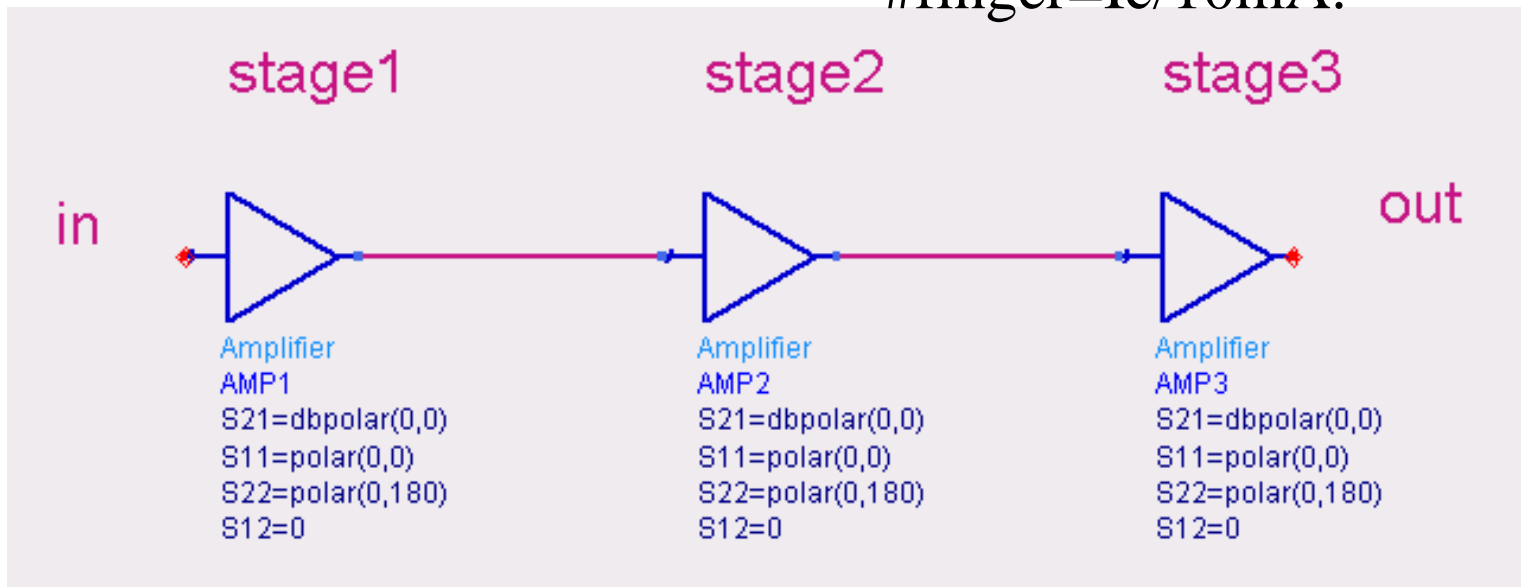


# Sizing Transistors in a Multistage PA

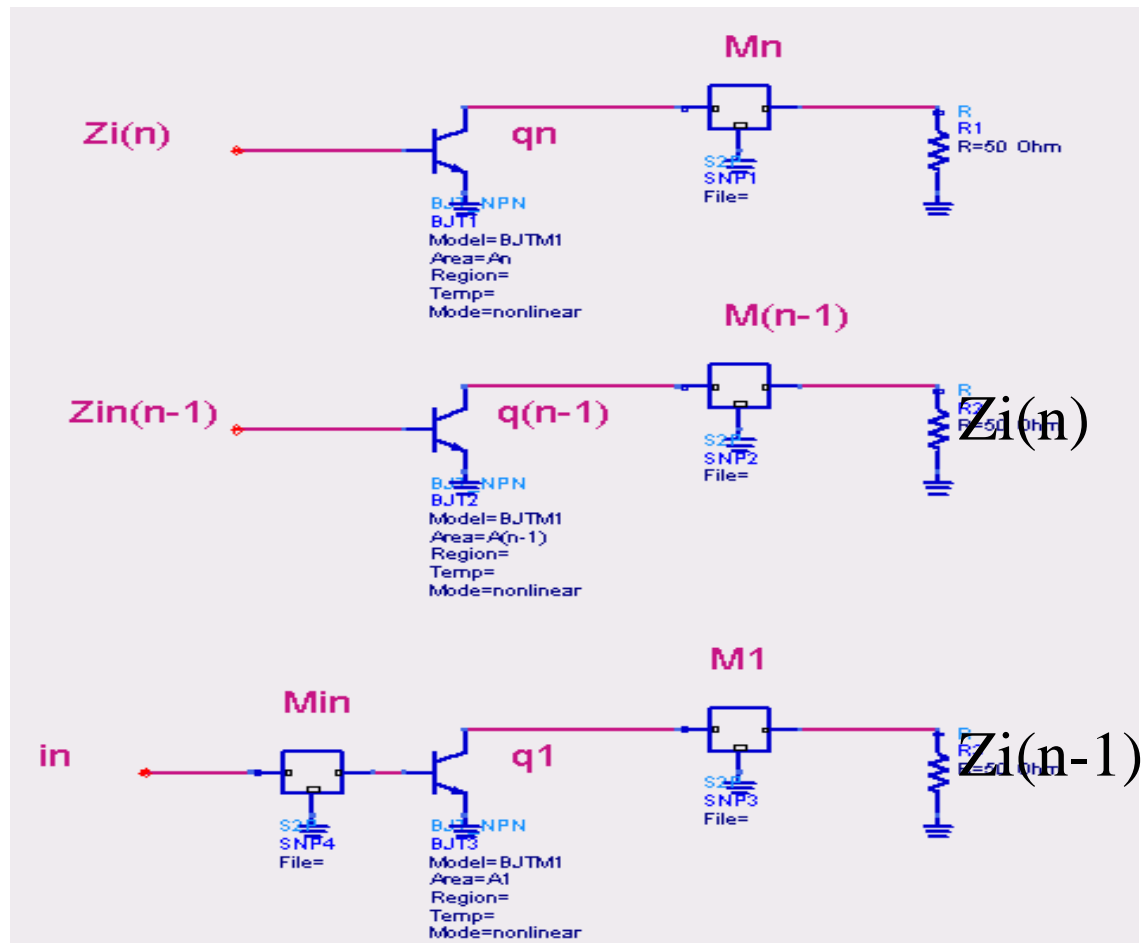
For each stage:

$$I_c = P_o / V_{cc}(\text{eff})$$

$$\# \text{finger} = I_c / 10 \text{mA}$$



# Matching Process for PA's, Starting at the Output



# PA Interstage Power and OIP3 Spreadsheet

STAGE	GAIN	POWER	OIP3
N	G(N)	$P_o$	OIP3
N-1	G(N-1)	$P_o \cdot G(N)$	OIP3-G(N)
N-2	G(N-2)	$P_o \cdot G(N) \cdot G(N-1)$	OIP3-G(N)-G(N-1)
N-3	G(N-3)	$P_o \cdot G(N) \cdot G(N-1) \cdot G(N-2)$	OIP3-G(N)-G(N-1)-G(N-2)
1	G(1)	$P_o \cdot G(N) \cdot G(N-1) \cdot G(N-2) \cdot \dots \cdot G(2)$	OIP3-G(N)-G(N-1)-G(N-2)-\dots-G(2)

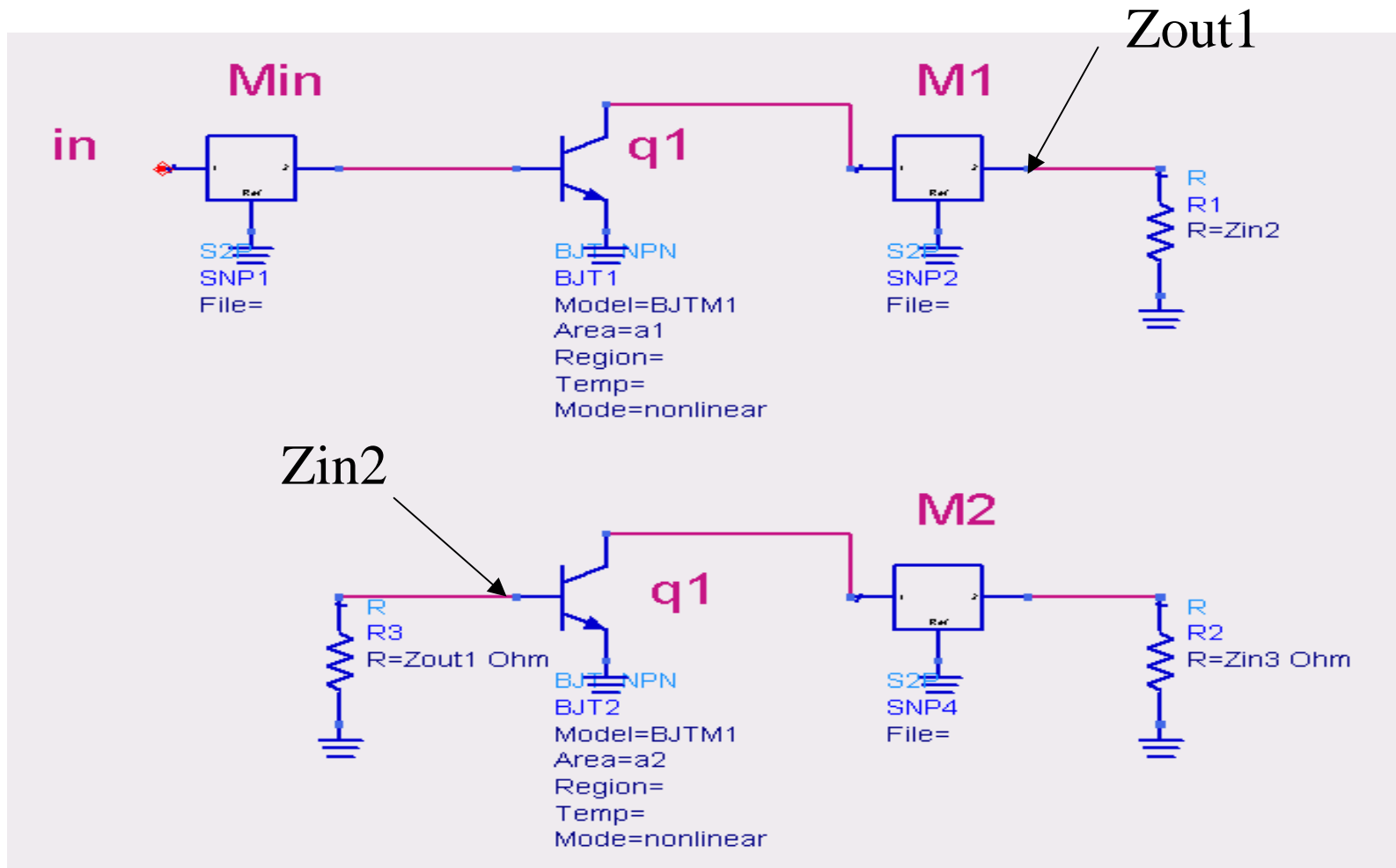
# PA Interstage Parameter Spreadsheet

STAGE	RL	P <sub>o</sub>	OIP3	GAIN	SIZE	I <sub>c</sub>
N						
N-1						
N-2						
N-3						
	1					

# Multistage PA Design Procedure

- Based on estimated stage gain, determine the Power output and OIP3 for each stage.
- Based on estimated efficiency, determine the DC current of each stage (I.e.  $P_{out} = (\text{eff})(V_{cc})(I_c)$  ). Size each stage based on DC current (I.e. assume 10 mA per finger)
- Use load line resistance to determine  $R_l$  for each stage (I.e. at 3 volt operation,  $R_l = 225 / (N_{\text{fingers}})$ ).
- Synthesize interstage matching networks which provide the correct  $R_l$  for each stage.

# Matching Process for LNAs: Start at Input



# Multistage LNAs design procedure

- Match stage1 to the 50 Ohm input resistance to give minimum stage1 noise figure.
- Match stage2's input to stage 1's output, in order to achieve minimum stage2 noise figure.
- Matching for noise need only be accomplished for the first two stages. After stage2, the “second stage” contribution of each stage is minimized.

Design Example: .5 watt output,  
two stage, 10 dB gain per stage,

## 50% Efficiency

- Output power of stage one is .050 watts.
- Output power of stage two is .50 watt.
- Assuming 3 volt operation,  $I_c$  for stage2 is  $(.5\text{watt}/3(50\%))=330$  mA,  $\text{size}=330/10=33$  fingers,  $R_l=225/33$  Ohms.
- Assuming 3 volt operation,  $I_c$  for stage1 is  $(.05/3(50\%))=33$  mA,  $\text{size}=33/10=3.3$  fingers,  $R_l=225/3.3$  Ohms.